Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claims 1-6 (cancelled).

Claim 7 (previously presented): The test configuration according to claim 20, including a radiation-absorbing layer disposed between said solar cell and said semiconductor chip.

Claims 8-19 (cancelled).

Claim 20 (currently amended): A test configuration, comprising:

a semiconductor wafer having a surface with an area;

a plurality of semiconductor chips disposed on said surface of said semiconductor wafer, each of said semiconductor chips having a self-test unit generating test information for functionally checking said semiconductor chip, said plurality of semiconductor chips having top surfaces; and

an energy source disposed above said semiconductor wafer and connected to said semiconductor chip for providing an

electrical energy supply to said semiconductor chip, said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly, said solar cell being disposed ~~areally~~ entirely over said area of said surface of said semiconductor wafer and over said top surfaces of said semiconductor chips.

Claim 21 (previously presented): The test configuration according to claim 20, including a radiation-absorbing layer between said solar cell and said semiconductor wafer, said radiation-absorbing layer having an electrically conductive plated-through hole formed therein disposed between said solar cell and said semiconductor chip.

Claim 22 (previously presented): The test configuration according to claim 21, wherein said radiation-absorbing layer has a pn junction disposed along said plated-through hole at a boundary between said plated-through hole and said radiation-absorbing layer for preventing a current flow between said plated-through hole and a remainder of said radiation-absorbing layer.

Claim 23 (previously presented): The test configuration according to claim 20, wherein said semiconductor chip has a

functional unit for a contactless transmission of data containing information about a test result.

Claim 24 (previously presented): The test configuration according to claim 23, including a receiver disposed separate from said semiconductor chip, said functional unit having an output terminal through which the data to be transmitted can be transmitted by capacitive coupling to said receiver.

Claim 25 (previously presented): The test configuration according to claim 23, wherein said semiconductor chip has a detector selected from the group consisting of voltage detectors and current detectors, said detector is connected to said energy source and to said functional unit for initiating a data transmission by said functional unit due to a detected characteristic voltage sequence or current sequence.

Claim 26 (previously presented): The test configuration according to claim 20, wherein said semiconductor chip has a terminal and a nonvolatile memory unit for storing data containing information about a test result, said nonvolatile memory unit being connected to said terminal through which the data of said nonvolatile memory unit can be tapped off to a point outside said semiconductor chip.

Claim 27 (previously presented): The test configuration according to claim 20, wherein one of said semiconductor chips is decoupled from respective others of said semiconductor chips with regard to said energy supply during a functional test.

Claim 28 (previously presented): The test configuration according to claim 20, wherein all of said semiconductor chips to be tested are connected to said energy source being a common energy source, each of said semiconductor chips has a current limiter circuit for electrically isolating a respective semiconductor chip from said common energy source in an event of a limit value of an operating current being exceeded.

Claim 29 (previously presented): The test configuration according to claim 20, wherein each of said semiconductor chips has an integrated memory containing memory cells to be subjected to a functional test, and said self-test unit generates test information and carries out a functional test of said memory cells.

Claim 30 (previously presented): The test configuration according to claim 29, wherein said integrated memory has normal memory cells and redundant memory cells for replacing

said normal memory cells, and said self-test unit is configured for checking a functionality of said normal memory cells, for analyzing which of said normal memory cells are to be replaced by which of said redundant memory cells, and for activating said redundant memory cells in accordance with a result of the analysis.

Claim 31 (previously presented): The test configuration according to claim 30, wherein said integrated memory has electrically programmable memory units for activating said redundant memory cells, in which a repair result determined by said self-test unit can be programmed.